SCHEME OF EXAMINATION

M.Tech. (VLSI Design)
Regular Programme

FIRST SEMESTER EXAMINATION

Code No.	Paper	L	T/P	Credits	Page no. of Syllabus
Theory Papers					
MEVS-601	Digital System Design using Verilog	4	-	4	209
MEVS-603	VLSI Technology	4	-	4	210
MEVS -605	Advanced VLSI Design	4	-	4	212
Electives (Choose any TWO)					
MECS-607	Advanced Computer Architecture	4	-	4	56
MEVS-609	Algorithm Analysis and Design	4		4	215
MEVS-611	DSP for VLSI Design	4	-	4	217
MECS- 611	Computational Techniques using MATLAB	4	-	4	58
MEVS-613	Wireless Networks	4		4	219
MEVS-615	Research Methodologies	4		4	221
Practical / Viva Voce					
MEVS-651	Lab-1 (DSD Lab)	-	2	1	225
MEVS-653	Lab-2 (VLSI Tech. Lab)	-	2	1	225
MEVS-655	Lab-3 (Ad. VLSI Lab)	-	2	1	225
MEVS-657*	Term Paper – I			2	225
Total		**20**	**6**	**25**	

*** NUES : Non University Examination**

SCHEME OF EXAMINATION

M.Tech. - (VLSI Design)
Regular Programme

SECOND SEMESTER EXAMINATION

Code No.	Paper	L	T/P	Credits	Page no. of Syllabus
MEEC-618	ESD Using ARM microcontroller	4	-	4	126
MEVS-604	Analog VLSI Design	4	-	4	211
MEVS-606	Low Power VLSI Design	4	-	4	213
Electives (Choose any two)					
MEVS-608	Advanced DSP for VLSI Design	4	-	4	214
MEVS-610	Simulation and Circuit Modeling.	4	-	4	216
MEVS-612	System on Chip	4	-	4	218
MEVS-614	Semiconductor Memory Design	4	-	4	220
MEVS-616	Evolutionary Algorithms for VLSI Design	4	-	4	222
MEVS-618	Secured Hardware Design	4	-	4	223
MEVS-620	Probability and Stochastic Processing	4	-	4	224
MESP-612	Digital Image Processing	4	0	4	170
Practical/Viva voce					
MEVS-652	Lab-4 (ESD Lab)	-	2	1	226
MEVS-654	Lab-5 (AVLSI Lab)	-	2	1	226
MEVS-656	Lab-6 (LPVLSI Lab)	-	2	1	226
MEVS-658*	Term Paper II	-	-	2	226
Total		**20**	**6**	**25**	

*** NUES : Non University Examination**

SCHEME OF EXAMINATION

M.Tech. - (VLSI Design)

Regular Programme

THIRD SEMESTER EXAMINATION

Code No.	Paper	L	T/P	Credits	Page no. of syllabus
MEVS-701	Algorithm for VLSI Physical Design Automation	4	-	4	227
MEVS-703	VLSI Design Test and Testability	4	-	4	228
Electives (Choose any THREE)					
MEVS-705	Analog-Mixed Signal Design	4	-	4	229
MEVS-707	Hardware-Software Co-design	4	-	4	230
MEVS-709	Designing with FPGA	4	-	4	231
MEVS-711	Advanced Digital Communication System	4	-	4	232
MEVS-713	MEMS and IC Integration	4	-	4	233
MEVS-715	Network on Chip Design	4	-	4	234
MEVS-717	CMOS RF Design	4	-	4	235
MEVS-719	Circuit Interconnections and Packaging for VLSI	4	-	4	236
MEEC-705	Embedded Systems & RTOS	4	-	4	132
Practical/viva voce					
MEVS-751	Lab-7 (Algo. VLSI PDA Lab)	-	2	1	237
MEVS-753	Lab-8 (VDTT Lab)	-	2	1	237
MEVS-755*	Term Paper III	-	2	2	237
MEVS-757	Minor Project	-	-	4	237
Total		**20**	**6**	**28**	

*** NUES : Non University Examination**

SCHEME OF EXAMINATION

M.Tech. - (VLSI Design)
Regular Programme

FOURTH SEMESTER EXAMINATION

Code No.	Paper	L	T/P	Credits
MEVS-752	Dissertation	-	-	24
MEVS-754*	Seminar & Progress Report	-	-	4
MEVS-756*	Term Paper-IV	-	-	2
	Total	-	-	30

***Non University Exam System**

NOTE:

3. The total number of credits of the Programme M. Tech. = 108.
4. Each student shall be required to appear for examination in all courses. However, for the award of the degree a student shall be required to earn the minimum of 100 credits (Elective Courses may be dropped only)

Paper Code: MEVS - 601	**L**	**T**	**C**
Paper: Digital System Design with Verilog	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit-1

ASIC Design Flow, Architecture and configuration of (Xilinx)Virtex series FPGA, Principles Hardware Description Languages, Y-Chart, Review of Synchronous and Asynchronous Design, Types of HDLs, Introduction to Verilog, Language Constructs ,Modeling style, Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators,

Unit-2

Design of Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter. Behavioral Modeling: Functional Bifurcation, Initial & Always Construct, multiple always blocks, Program flow control and looping, Parallel blocks, force-release construct, design of sequential circuits using verilog: Register, Counters, Timing and Delays model, path delay modeling, timing check

Unit 3

Introduction of behavioral modelling, functional bifurcation, initial & always construct, procedural assignment statement, Delay in Procedural statements, Timing Control Statements, If and If-else, case statement assign-deassign, repeat construct, loop construct: repeat, for, while & forever, sequential and parallel blocks, force-release construct, design of flip flop, shift register and counters using Verilog

Unit-4

Data Subsystems, Storage Modules, Functional Modules, Data paths, Control Subsystems, Micro programmed Controller, Structure of a micro programmed controller, Micro instruction Format, Micro instruction sequencing, Micro instruction Timing, Basic component of a micro system, memory subsystem design.

Text Books:

[1] Verilog HDL by Samir Palnitkar, Pearson Pub.
[2] M. Ercegovac, T. Lang and L.J. Moreno, "Introduction to Digital Systems", Wiley,2000

Reference Books:

[1] Digital Design by Frank Vahid, Wiley, 20063.
[2] Introduction to Digital Systems by M. Ercegovac, T. Lang and L.J. Moreno, Wiley,2000.
[3] Fundamental of digital Logic with Verilog design by S. Brown & Z. Vransesic, TMH.
[4] Design through Verilog HDL by T.R. Padmanabhan& B. Bala Tripura Sundari, Wiley Pub. 2007

Paper Code: MEVS-603	**L**	**T**	**C**
Paper: VLSI Technology	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Cleanroom technology - Clean room concept – Growth of single crystal Si, surface contamination, Chemical Mechanical Polishing, wafer preparation, DI water, RCA and Chemical Cleaning. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc.

Epitaxy : Physical Vapour Deposition, Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Unit 2

Oxidation :Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO_2.

Diffusion :Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, Ion Implantation, Annealing and diffusion from an ion implanted layer.

Unit 3

Lithography

Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.

Unit 4

Etching

Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching.

Metallisation - Different types of metallization, uses & desired properties

Text Books

[1] S.M. Sze, " VLSI Technology", John Wiley & Sons, 2000.

Reference Books

[1]B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.

[2] Wai-Kai Chen,"VLSI Technology" Wiley, March 2003.

Paper Code: MEVS – 604	**L**	**T**	**C**
Paper: Analog VLSI Design	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction to analog design - Levels of abstraction, Robust analog design, MOS Device Models, MOS Device Capacitances, MOS small signal model, long channel vs. short channel, Single stage amplifier- Basic concepts, Common Source Stage, Source follower, Common Gate stage, Cascode Stage

Unit 2

Differential amplifiers - Single ended and Differentials Operation, Common Mode Response Differential pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic current mirrors, Cascode Current Mirrors, Active Current Mirrors. Frequency Response of Amplifiers – General Considerations, CS stage, Source Followers, CG stage, Cascode stage, Differential Pair. Feed Back – General Considerations, Feedback Topologies, Effect of Loading.

Unit 3

Operational Amplifiers – General Considerations, One stage and two stage Op Amps, Gain boosting, Comparison, Common-mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Stability and Frequency compensations – General Considerations, Multipole System, Phase Merging, Frequency Compensation, and Compensation of Two Stage Op-Amp.

Unit 4

Voltage controlled oscillator, Phase Locked Loops (PLL) – Simple PLL, Charge Pump PLLs, Introduction to Switched - Capacitor Circuits – General Considerations, Sampling Switches, , Switched Capacitor Amplifiers, Switched Capacitor Integrator, Switched Capacitor Common Mode Feedback.

Text Books:

[T1] Design of Analog CMOS integrated circuits Behzad Razavi McGraw-Hill International edition - ISBN-0-07-118815-0, 2001

[T2] Analog integrated circuit Design, David A. Johns & Ken Martin - John- Wiley & Sons, Inc. New York. ISBN-0-471-14448-7

Reference Books :

[R1] CMOS: Circuit Design, layout, and simulation, R. Jacob, Baker and David E. Boyce, Prentice Hall of India. ISBN - 81-203-1682-7

[R2] Applications and Design with analog integrated circuits, 2 nd Edition - J. Michael Jacob, Prentice Hall of IndiaISBN-81-203-1015-2

[R3] Design and applications of analog Integrated Circuits, Sidney Soclof , Prentice Hall of India, -ISBN - 81 - 203 - 2 55 2 - 4 , 1991

Paper Code: MEVS-605	**L**	**T**	**C**
Paper: Advanced VLSI Design	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

3. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
4. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction [T1,T2]: Basic principle of MOS transistor, Introduction to large signal MOS models (long channel) for digital design.

MOS Circuit Layout & Simulation and manufacturing: scaling, MOS SPICE model and simulation, CMOS layout: design rules, Transistor layout, Inverter layout, NMOS and CMOS basic manufacturing steps.

Unit 2

The MOS Inverter [T1]: Inverter principle, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, switching characteristics, Propagation Delay, Power Consumption.

Combinational MOS Logic Design [T1] : Static MOS design, Ratioed logic, Pass Transistor logic, complex logic circuits.

Unit 3

Sequential MOS Logic Design [T1]

Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Astable Circuits. Memory Design: ROM & RAM cells design **Dynamic MOS design [T1]:** Dynamic logic families and performances.

Clock Distribution [T1] [T2]Clock Distribution. Input and Output Interface circuits.

Unit 4

Subsystem design [T2, R1]

Design styles, design concepts: Hierarchy, Regularity, Modularity, Locality. CMOS Sub system design: Adders, Multipliers.

Text Books

[T1] S. Kang & Y. Leblebici "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003.

[T2] J. Rabaey, "Digital Integrated Circuits Design", Pearson Education, Second Edition, 2003.

Reference Books

[R1] Neil Weste and David Harris :" CMOS VLSI design" Pearson Education 2009.

Paper Code: MEVS-606	L	T	C
Paper: Low Power VLSI Design	4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit-1

Introduction[T1] [T2]: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power [R1]: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. Power estimation Techniques

Unit 2

Simulation Power analysis [T1]: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Unit 3

Low Power Techniques[T1] : Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Unit 4

Low power Architecture & Systems[T1] Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution[T2]: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

Text Books:

[T1] Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
[T2] Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

Reference Books:

[R1] Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.

Paper Code: MEVS-608	L	T	C
Paper: Advanced DSP for VLSI Design	4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1: DISCRETE RANDOM SIGNAL PROCESSING

Discrete Random Processes, Expectations, Variance, Co -Variance, Scalar Product, Energy of Discrete Signals - Parseval's Theorem, Wiener Khintchine Relation - Power Spectral Density - Periodogram – Sample Autocorrelation - Sum Decomposition Theorem, Spectral Factorization Theorem - Discrete Random Signal Processing by Linear Systems - Simulation of White Noise - Low Pass Filtering of White Noise

Unit 2 : SPECTRUM ESTIMATION

Non-Parametric Methods-Correlation Method - Co-Variance Estimator - Performance Analysis of Estimators - Unbiased, Consistent Estimators-Periodogram Estimator-Barlett Spectrum Estimation-Welch Estimation-Model based Approach - AR, MA, ARMA Signal Modeling-Parameter Estimation using Yule-Walker Method.

Unit 3: LINEAR ESTIMATION AND PREDICTION

Maximum likelihood criterion-efficiency of estimator-Least mean squared error criterion -Wiener filter-Discrete Wiener Hoff equations-Recursive estimators-Kalman filter-Linear prediction, prediction error-whitening filter, inverse filter-Levinson recursion, Lattice realization, and Levinson recursion algorithm for solving Toeplitz system of equations.

Unit 4: ADPATIVE FILTERS

FIR adaptive filters-Newton's steepest descent method - adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm- Adaptive channel equalization-Adaptive echo chancellor-Adaptive noise cancellation-RLS adaptive filters-Exponentially weighted RLS-sliding window RLS-Simplified IIR LMS adaptive filter

MULTIRATE DIGITAL SIGNAL PROCESSING

Mathematical description of change of sampling rate - Interpolation and Decimation - continuous time model - Direct digital domain approach - Decimation by an integer factor - Interpolation by an integer factor - Single and multistage realization - poly phase realization - Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

Text Book:

[T1] Monson H.Hayes, " Statistical Digital Signal Processing and Modeling ", John Wiley and Sons, Inc., New York, 1996.

Reference Books:

[R1]. Sopocles J.Orfanidis, " Optimum Signal Processing ", McGraw Hill, 1990.
[R2]John G.Proakis, Dimitris G.Manolakis, " Digital Signal Processing ", Prentice Hall of India, 1995

Paper Code: MEVS-609	**L**	**T**	**C**
Paper: Algorithm Analysis and Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction to Algorithm, The role of algorithms in computing, Asymptotic notation, asymptotic analysis of recurrence relations, probabilistic analysis and randomized algorithm, the hiring problem, indicator random variables, Divide and conquer paradigm – Merge sort, Inversion counting, Dynamic Programming – Matrix Chain multiplication, Longest Common subsequence, optimal binary search trees Greedy Algorithm –Activity Selection problem, Theoretical foundation of greedy algorithm, Task Scheduling problem, Comparison of dynamic programming and Greedy algorithm with Knapsack as case study

Unit 2

Graphs: Review of Graphs (Representation, Depth First Search, Breath First search, Kruskal and Prim Algorithm, Dijkstra's Algorithm) Flow networks: Ford-Fulkerson method, comparison Networks, Zero-one Principle, Bitonic Sorting Network, Merging Network, Sorting Network

Unit 3

Matrix Operation (Properties, Strassen's Algorithm, Solution of linear equation, Matrix inversion) Polynomial and FFT, Representation of polynomials, The DFT and FFT, efficient FFT implementation Number–Theoretic Algorithm, Elementary number-theoretic notion, Greatest common divisor, modular arithmetic, solving modular linear equation, the Chinese remainder theorem

Unit 4

NP-Completeness, Polynomial time, Polynomial time verification, NP completeness and reducibility, NP-Completeness proofs Approximation Algorithms- the vertex-cover problem, Traveling-Salesman Problem, set covering problem

Text Books:

[T1] T. H. Cormen, C. E. Leiserson, R.L. Rivest, C. Stein, "Introduction to Algorithms", 2nd Edition, PHI.

Reference Books:

[R1] A.V. Aho, J. E. Hopcroft, J.D. Ulman, "The Design & Analysis of Computer Algorithms", Addison Wesley.
[R2] V. Manber, "Introduction to Algorithms – A Creative Approach", Addison Wesley.
[R3]Ellis Harwitz and Sartaz Sahani, "Fundamentals of Computer Algorithms", Galgotia.

Paper Code: MEVS - 610	**L**	**T**	**C**
Paper: Simulation and Circuit Modeling	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1[T1]

Introduction, Main data structure & program organization, Geometrical manipulations, Ion implantation. .

Unit 2 [T1]

A novel measurement technique for 2D implanted ion distributions, Introduction to partial differential equation solver.

Unit 3 [T1]

The merged multi grid method, Isothermal device modeling & simulation. .

Unit 4 [T1]

Non-Isothermal device modeling & simulation, hydrodynamic device modeling & simulation.

Text Books

[T1] Circuit, Device and Process Simulation: Mathematical and Numerical Aspects by Graham F. Carey (Editor), W. B. Richardson, C. S. Reed, B. Mulvaney, John Wiley & Sons; 1st edition. 1996.

Reference Books:

[R1] Process and Device Simulation for MOS-VLSI Circuits, edited by P. Antognetti, D.A. Antoniadis , Robert W. Dutton, W.G. Oldham, Kluwer Academic Publisher, 2000.

Paper Code: MEVS – 611	**L**	**T**	**C**
Paper: DSP for VLSI Design	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1: VLSI DSP

Data Flow graph representation, Iteration Bound, Pipelining and Parallelism; Re-timing techniques, Unfolding-algorithm, properties and applications of unfolding, Folding transformation, register minimization in folded architectures, folding of multirate systems

Unit 2: Architecture Design

DSP system architectures, Systolic Array Design Methodology, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit serial PEs. Pipelined and Parallel Architectures for Recursive and Adaptive Filters

Unit 3 : Arithmetic Architectures

Bit level arithmetic architectures, redundant arithmetic, synchronous and asynchronous pipeline, low power design

UNIT 4: Case Study: TMS320CXX PROCESSOR

Architecture –Data formats, Addressing modes, Instruction sets and operations, Block diagram of DSP starter kit, Programs for processing real time systems

Text Book

[T1] K. K. Parhi, VLSI Digital Signal Processing Systems : Design and Implementation, Wiley,1999
[T2] B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" -Tata McGraw Hill Publishing Company Limited. New Delhi, 2008

Reference Books:

[R1] P. Lapsley, J. Bier, A. Shoham and E. A. Lee, DSP Processor Fundamentals : Architectures and Features, Wiley/IEEE,2001.
[R2] P. Pirsch, Architectures for Digital Signal Processing, Wiley, 1998.
[R3] T. Glokler and H. Meyr, Design of Energy-Efficient Application Specific Instruction Set Processors, Kluwer, 2004.
[R4] V. K. Madisetti, VLSI Digital Signal Processors, Butterworth-Heinemann/IEEE Press, 1995.

Paper Code: MEVS - 612	**L**	**T**	**C**
Paper: System-on-chip	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT-1

Logic Gates

Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect.

Unit-2

Combinational Logic Networks.

Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay. Logic and Interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

Sequential Machines.

Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines. Sequential System Design. Power Optimization. Design Validation. Sequential Testing.

Unit-3

Subsystem Design

Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. Field-Programmable Gate Arrays. Programmable Logic Arrays. References. Problems.

Unit-4

Floor-planning

Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, Switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, The I/O Architecture, PAD Design.

Text Book:

[T1] Wayne Wolf , " Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition , 2008.

Reference Book:

[R1] Wayne Wolf , " Modern VLSI Design – IP based Design", Prentice Hall, 4th Edition , 2008.

Paper Code: MEVS – 613	**L**	**T**	**C**
Paper: Wireless Networks	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction to Personal Communication Services (PCS): PCS architecture, Mobility management, Networks signaling.

Global system for Mobile Communication (GSM) system overview: GSM Architecture, Mobility Management, Network signaling.

Unit 2

General Packet Radio Services (GPRS): GPRS architecture, GPRS Network nodes. Enhanced Data rates for GSM Evolution (EDGE), Mobile Data Communication: WLANs (Wireless LANs) IEEE 802.11 standard, Mobile IP. Wireless Application Protocol (WAP): The Mobile Internet standard, WAP Gateway and Protocols, Wireless Markup Languages (WML).

Unit 3

Third Generation (3G) Mobile Services: Introduction to International Mobile Telecommunications 2000 (IMT 2000) vision, Wideband Code Division Multiple Access (W-CDMA), and CDMA 2000, Quality of services in 3G. Fourth Generation (4G) Mobile services: Introduction to Long Term Evaluation (LTE), Orthogonal Frequency Division Multiple Access (OFDMA), Multi-In Multi-Out Antenna system (MIMO), LTE-Advanced Wireless local Loop (WLL): Introduction to WLL architecture, WLL technologies, WMAN (Wireless MAN), IEEE802.16 standard, WiMAX

Unit 4

Global Mobile Satellite Systems: Case studies of IRIDIUM and GLOBALSTAR systems.

Bluetooth technology. Wireless Sensor Networks: Introduction, Architecture, ZigBee protocol, Applications.

Text Books:

[T1] Yi –Bing Lin & Imrich Chlamatac ,"Wireless and mobile Networks Architecture," John Wiley & Sons Publication, 2001.

[T2] Raj Pandya, "Mobile & Personnel communication Systems and Services", Prentice Hall India, 2001.

[T3] Theodore S. Rappaport, "Wireless Communication- Principles and practices," 2nd Ed. Pearson Education Pvt. Ltd, 2003.

[T4] Jochen Schiller, "Mobile communications," Pearson Education Pvt. Ltd., 2002.

[T5] Singhal & Bridgman, " The Wireless Application Protocol," Pearson Education, 2004.

References Books :

[R1] Hensmann, Merk, & Stober, "Principles of Mobile Computing," 2nd Ed., Springer International Edition, 2003.

[R2] Talukdar & Yaragal, "Mobile Computing," TMH, 2005.

[R3] Smith & Collins, "3G Wireless Networks," TMH, 2007.

Paper Code: MEVS - 614	**L**	**T**	**C**
Paper: Semiconductor Memory Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit-1

Introduction to Advanced Semiconductor Memories – Overview, Developments & Directions. SRAM Technologies – Basic SRAM Architecture & Cell Structures, SRAM selection Considerations, High Performance SRAMs, Advanced SRAM Architectures.

Unit-2

Low Voltage SRAMS, SOI SRAMS, BiCMOS SRAM, CAM. Memory Peripheral Circuitry – The Address Decoder, Sense Amplifier, Voltage References, Drivers / Buffers, Timing & Control, Memory Reliability & Yield. Power Dissipation in Memories – Sources of Power Dissipation, Partitioning of the Memory, Addressing the active power dissipation, Data Retention Dissipation.

Unit-3

DRAM – Technology & Evolution & Trends, DRAM Timing Specifications, EDO DRAMs, EDRAM, Synchronous DRAM, Enhanced Synchronous DRAM, Cache DRAM.

Unit-4

NON VOLATILE MEMORY – Introduction, Floating Gate cell Theory & Operations, Charge Transport Mechanisms, and Nonvolatile Memory Cell & Array Design, UV-EPROM cells & EEPROM Cells, Flash Memory Cells.

Flash Memory Architectures – NOR, NAND, DINOR & AND Architecture Flash Memories. Multilevel Nonvolatile Memories, Ferroelectric Memories.

Text Books:

[T1] Ashok K Mishra , "Advanced Semiconductor Memories", IEEE Press, Wiley & Sons, 2009.

[T2] Jan M .Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd edition Prentice Hall Publication, 2011

Reference Books:

[R1] S. Kang & Y. Leblebici "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003.

[R2] Betty Prince, "Semiconductor Memories: A Handbook of Design, Manufacture and Application", John Wiley & Sons Publication.

Paper Code: MEVS – 615	**L**	**T**	**C**
Paper: Research Methodologies	**4**	**-**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

3. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
4. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1: Introduction to Research Methodology

Meaning of research, objectives of research, meaning of research, motivation in research, types of research, scope of educational research, characteristics and prerequisites of educational research, types of educational research, research approaches, significance of research, research methods versus methodology, research and scientific method, importance of knowing how research is done, research process, criteria of good research, necessity of defining the problem.

Unit II: Techniques for Research Methodology

Defining research problems, hypothesis formulation, developing a research plan, research design, features of a good design, different research designs, and important concepts related to research design, methods for data collection.

Unit III: Data Analysis and Statistical Techniques

Data and their analyses, quantitative methods and techniques, Measure of central tendency, measures of variation, frequency distribution, analysis of variance methods, identifying the distribution with data, parameter estimation, Goodness-of-Fit tests-Chi-Square test, K-S Goodness-of-Fit test, Correlation analysis, Regression analysis, time series and forecasting, Introduction to discriminate analysis, factor analysis, cluster analysis, conjoint analysis. Sampling methods, test of hypothesis

Unit IV : Algorithmic Research and Simulation

Algorithmic research problems, types of algorithmic research, types of solution procedure, steps of development of algorithm, steps of algorithmic research, design of experiments, steps of modeling, operations research models, application of models. Need for simulation, types of simulation, simulation language, fitting the problem to simulation study, simulation models, output analysis.

Books:

[R1]Research Methodologies, R. Panneerselvam, Prentice Hall, 2007.
[R2] Research in Education, Best John V. and James V Kahn, Wiley eastern, 2005.
[R3] Elements of Educational Research, Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra, PHI publication, 2003.
[R4] Methodology of Research Education, K. Setia, EEE publication, 2004.
[R5] Research methodology, Methods and Techniques, Kothari, C.R., 2000.

Paper Code: MEVS - 616	**L**	**T**	**C**
Paper: Evolutionary Algorithms for VLSI Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Logic synthesis & verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis, Basic VLSI automation Algorithms: Partitioning, Placement, floor planning & pin assignment, routing.

Unit 2

Basic Principles of Evolutionally Algorithms, Mutually dependent problems, Heuristic minimization, CAD of IC, Biological background, Genetic algorithm and Evolutionary algorithms, Extension of the concept.

Unit 3

Characteristics of Problem instances: Size of problem instance, Quality speed trade-off, Performance evaluations: Measuring performance, Design space exploration, Quality versus Speed

Unit 4

EA Tools, GAME: The Environment, Applications, Applications of EAS: Logic synthesis, mapping, testing, guidelines for CAD applications, Heuristic Learning: The learning model, Minimization of decision diagrams

Text Books:

[T1] Evolutionary Algorithms for VLSI CAD , Rolf Drechsler Springer; 1st edition (May 31, 1998)

Reference Books:

[R1] Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
[R2] Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002.

Paper Code: MEVS - 618	**L**	**T**	**C**
Paper: Secured Hardware Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction to security attacks, services and mechanism, introduction to cryptography. Conventional Encryption: Conventional encryption model, classical encryption techniques- substitution ciphers and transposition ciphers, cryptanalysis, stereography, stream and block ciphers. Modern Block Ciphers: Block ciphers principals, Shannon's theory of confusion and diffusion, fiestal structure, data encryption standard(DES), strength of DES, differential and linear crypt analysis of DES, block cipher modes of operations, triple DES, IDEA encryption and decryption, strength of IDEA, confidentiality using conventional encryption, traffic confidentiality, key distribution, random number generation.

Unit 2

Introduction to graph, ring and field, prime and relative prime numbers, modular arithmetic, Fermat's and Euler's theorem, primarily testing, Euclid's Algorithm, Chinese Remainder theorem, discrete logarithms. Principals of public key crypto systems, RSA algorithm, security of RSA, key management, Diffle-Hellman key exchange algorithm Elganel encryption.

Unit 3

Message Authentication and Hash Function: Authentication requirements, authentication functions, message authentication code, hash functions, birthday attacks, security of hash functions and MACS, MD5 message digest algorithm, Secure hash algorithm(SHA).Digital Signatures: Digital Signatures, authentication protocols, digital signature standards (DSS), proof of digital signature algorithm.

Unit 4

Introduction to elliptic curves: Weierstrass equation, group law, projective space and points at infinity, elliptic curve in different characteristics, other models. Elliptic curve cryptography: elliptic curve-based Diffie-Hellman, El Gamal and Digital Signature Algorithm

Text Books:

[T1] William Stallings, "Cryptography and Network Security: Principals and Practice", Prentice Hall, New Jersy.

Reference Books

[R1] Johannes A. Buchmann, "Introduction to Cryptography", Springer-Verlag.
[R2] . Bruce Schiener, "Applied Cryptography".

Paper Code: MEVS - 620	**L**	**T**	**C**
Paper: Probability and Stochastic processing	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1: Introduction to Probability and Stochastic Processing
Probability models, Algebra of events, probability axioms, conditional probability, aye"s rules, Bernoulli traits. Discrete Random Variables: Discrete random variables, probability mass functions, discrete distribution functions-Bernoulli, Binomial, geometric, Poisson, hyper geometric & uniform distributions, probability generating function.

Unit 2
Continuous Random variable: Exponential distribution, memory less property, application to reliability, hypo exponential, Erlang, Gamma, hyper exponential & Normal distributions, order statistics, distribution of sums.

Unit 3
Stochastic Process, Classification, Discrete and continuous time markov chain, Poisson process, renewal process, littles formula, Erlang Loss Model, M/M/1 Queue, M/M/m Queue Multidimensional Queue. Queueing Networks. Definitions and Notation. Performance Measures. Product-Form Queuing Networks. Algorithms for Product-Form Networks, priority Networks.

Unit 4
Solution Techniques: Steady-State Solutions of Markov Chains, Solution for a Birth Death Process, Matrix-Geometric Method: Quasi-Birth-Death Process, Heisenberg Matrix: Non-Markovian Queues, Transient analysis, stochastic Petri nets, Numerical Solution: Direct Methods, Numerical Solution: Iterative Methods, Comparison of Numerical Solution Methods, Performance Measures,

Text Book
[T1] Papoulis, A., Probability , Random Variables and Stochastic Processes, Third Edition, McGraw-Hill.

Reference Book
[R1] K.S Trivedi: Probability and Statistics, PHI, 3rd Ed.
[R2] S.P Gupta, Statistical Methods, Sultan Chand and Sons.
[R3] V.K Kapoor and S.C Gupta, Fundamentals of Statistics, Sultan Chand and Sons.

Code No: MEVS-651	**L**	**P**	**C**
Lab-1	**-**	**2**	**1**

Experiment of the lab will be based on Digital System Design with Verilog.

Code No. : MEVS-653	**L**	**P**	**C**
Lab-2:	**-**	**2**	**1**

Experiment of the lab will be based on VLSI Technology.

Code No: MEVS-655	**L**	**P**	**C**
Lab-3	**-**	**2**	**1**

Experiment of the lab will be based on advanced VLSI Design.

Code No: MEVS-657*	**L**	**P**	**C**
Term paper-1		**-**	**2**

Lab Experiment/Lab- project will be based on Elective/s/Research work

* Non University Exam

Code No: MEVS-652	**L**	**P**	**C**
Lab-1	**-**	**2**	**1**

Experiment of the lab will be based on ESD

Code No. : MEVS-654	**L**	**P**	**C**
Lab-2:	**-**	**2**	**1**

Experiment of the lab will be based on Analog VLSI Design.

Code No: MEVS-656	**L**	**P**	**C**
Lab-3	**-**	**2**	**1**

Experiment of the lab will be based on low power VLSI Design

Code No: MEVS-658*	**L**	**P**	**C**
Term paper-2		**-**	**2**

Lab Experiment/Lab- project will be based on Electives

- NUES: Non University Exam

Paper Code: MEVS - 701	**L**	**T**	**C**
Paper: Algorithm for VLSI Physical Design Automation	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

VLSI automation Algorithms[T1]:
Introduction, Physical design flow, Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution,

Unit 2
Placement, floor planning & pin assignment[T1]: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Unit 3
Global Routing[T1]: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms.
Detailed routing[T1]: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, switchbox routing algorithms.

Unit 4
Over the cell routing & via minimization[T1]: two layers over the cell routers constrained & unconstrained via minimization.
C**ompaction[T1]:** problem formulation, one-dimensional compaction, two dimension based compaction.

Text Books:

[T1] Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition, 2005.

***References** Books:*

[R1] Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.

[R2] Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition, 2002

[R3] Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Paper Code: MEVS - 703	**L**	**T**	**C**
Paper: VLSI Design Test and Testability	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction: The need for testing, the problems of digital and analog testing, Design for test, Software testing. **Faults in Digital circuits:** General introduction, Controllability and Observability, Fault Modeling- Logic, RTL and Structure level models, Compiled Simulation, Event- Driven Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate-Level Event- Driven Simulation, Simulation Engines. Fault models - Stuck-at faults, Bridging faults, intermittent faults.

Unit 2

Digital test pattern generation: Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing.

Unit 3

Signatures and self test: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients, Spectral coefficients, Coefficient test signatures, Signature analysis and Online self test.

Unit 4

Testability Techniques: Functional Testing- Basic Issues, Exhaustive, pseudo exhaustive testing, Partitioning and ad hoc methods and Scan-path testing, Testability – Ad-Hoc design for testability, Board level and System level DFT approach, Some advance scan concepts, BIST-memory BIST, Logic BIST, Hardware description languages and test.
Testing of Analog and Digital circuits: Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP.

Text Books

[1] VLSI Testing: digital and mixed analogue digital techniques. Stanley L. Hurst Pub:Inspec/IEE ,1999.
[2] M L Bushnell and V D Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits'", Springer, 2005.

Reference Books:

[1] Digital systems testing and testable design - Miron Abramovici et al , Computer Science Press (1991)
[2] Test generation for VLSI chips by VD Agrawal and SC Seth, IEEE Computer Society Press (2003) ISBN 0-8186-8786 -X.

Paper Code: MEVS - 705	**L**	**T**	**C**
Paper: CMOS Analog-mixed Signal design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Analog and discrete-time signal processing, introduction to sampling theory. Analog continuous-time filters: passive and active filters. Basics of analog discrete-time filters and Z-transform. Switched-capacitor filters. Non-idealities in switched-capacitor filters. Switched-capacitor filter architectures.

Unit 2

Basics of data converters: Successive approximation ADCs, Dual slope ADCs, High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), High-resolution ADCs (e.g. delta-sigma converters

Unit 3

DAC, Mixed-signal layout, Interconnects and data transmission, Voltage-mode signaling and data transmission, Current-mode signaling and data transmission, Introduction to frequency synthesizers and synchronization.

Unit 4

Basics of PLL, Analog PLL, Digital PLL, DLL,

Text / Reference Books:

1. CMOS mixed-signal circuit design by R. Jacob BakerWiley India, IEEE press, reprint 2008.
2. Analog Circuit design, layout and simulation by R. Jacob Baker Revised second edition, IEEE press, 2008.
3. Design of analog CMOS integrated circuits by Behad Razavi,McGraw-Hill, 2003.

Paper Code: MEVS - 707	**L**	**T**	**C**
Paper: Hardware/Software Codesign	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction [T1]: Motivation hardware & software co-design, system design consideration, research scope & overviews. Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development.

Unit 2

Hardware Software co-design research[T1]: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment. Co-design concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade offs, co-design.

Unit 3

Methodology for co-design[T1]: Amount of unification, general consideration & basic philosophies, a framework for co-design. Unified representation for Hardware & Software : Benefits of unified representation, modeling concepts. An abstract Hardware & Software model : Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model.

Unit 4

Performance evaluation[T1]: Application of t he abstract Hardware & Software model, examples of performance evaluation .Object oriented techniques in hardware design: Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.

Text Books:

[T1] Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Kluwer Academic Publisher, 2002.

Reference Books:

[R1] H. Kopetz, Real-time Systems, Kluwer, 1997.
[R2] R. Gupta, Co-synthesis of Hardware and Software for Embedded Systems, Kluwer 1995.
[R3] S. Allworth, Introduction to Real-time Software Design, Springer-Verlag, 1984.
[R4] Peter Marwedel, G. Goosens, Code Generation for Embedded Processors, Kluwer Academic Publishers, 1995.

Paper Code: MEVS – 709	**L**	**T**	**C**
Paper: Designing with FPGA	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

FPGA-Based Systems

Introduction, Basic Concepts, Digital Design and FPGAs, FPGA-Based System Design, Hardware Description Languages overview, The Logic Design Process, Logic Implementation for FPGAs.

Unit 2

FPGA Fabrics

Introduction, FPGA Architectures, SRAM-Based FPGAs, Permanently Programmed FPGAs, Chip I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics

Unit 3

Combinational Logic

Introduction, Combinational Network Delay, Power and Energy Optimization, Arithmetic Logic

Unit 4

Physical Design for FPGAs : Architecture- Introduction, Behavioral Design, Design Methodologies.
Large-Scale Systems : Introduction, Busses, Platform FPGAs, Multi-FPGA Systems, Novel Architectures

Text Book:

[T1] FPGA-Based System Design By: Wayne Wolf Publisher: Prentice Hall, 2004.

Reference Books:

[R1] Z Navabi, "Embedded Core design with FPGA", McGraw Hills, 1st edition, 2006.
[R2] Evgeni Stavinov, "100 power Tips for FPGA", OutputLogic.com (May 18, 2011)

Paper Code: MEVS - 711	**L**	**T**	**C**
Paper: Advance Digital Communication System	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1: Modulation Techniques

Digital Modulation Techniques :- Analysis, Generation and Detection (Block Diagram), Spectrum and Bandwidth of Amplitude Shift Keying (ASK), Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Offset and Non-offset Quadrature Phase Shift Keying (QPSK), M-ary PSK, Binary Frequency Shift Keying (BFSK), M-ary FSK, Minimum Shift Keying, Quadrature Amplitude Modulation (QAM), Comparison of digital modulation techniques on the basis of probability of error, Matched Filter.

Unit 2: Pulse Modulation

Sampling of Signal, Sampling Theorem for Low Pass and Band Pass Signals, Aliasing, Pulse Amplitude Modulation (PAM), Time Division Multiplexing (TDM), Channel Bandwidth for PAM-TDM Signal, Types of Sampling, Instantaneous, Natural and Flat Top Sampling, Aperture Effect, PPM and PDM techniques, Pulse Code Modulation (PCM), Signal-to-Noise Ratio in PCM, Companding, Data Rate and Bandwidth of Multiplexed PCM Signal, Inter-symbol Interference, Eye Diagram, Line Coding NRZ, RZ, Biphase,, Differential PCM (DPCM), Delta Modulation (DM), and Adaptive Delta Modulation (ADM), Slope Overload Error ,Granular Noise ,Comparison of various system in terms of Bandwidth and Signal-to-Noise Ratio.

Unit 3: Random Processes

Concept of Probability, Relative Frequency and Probability Conditional Probability and Independent Events, Random Variables, Discrete Random Variables, Cumulative Distribution Function(CDF), Probability Density Function(PDF),Statistical Averages (Means), Chebyshevs Inequality, Central Limit Theorem

Unit 4: Spread Spectrum Modulation

Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum with coherent binary phase shift keying, signal space dimensionality and processing gain, probability of error, frequency hop spread spectrum, maximum length and Golay codes.

Text Books:

[T1] B. Sklar, Digital Communication, Pearson Education.
[T2] Tomasi: Advanced Electronics Communication Systems, 6th Edition, PHI

References:

[R1] Taub & Schilling, Principles of Communication system, TMH.
[R2] Lathi B.P., Modern Analog and Digital Communication systems, Oxford Uni. Press.
[R3] Haykin Simon, Digital Communication, Wiley Publication.
[R4] Proakis, Digital communication, McGraw Hill
[R5] Schaum‟s Outline series, Analog and Digital Communication.
[R6] Singh and Sapre: Communication System, TMH
[R7] Couch: Digital and Analog Communication, Pearson Education
[R8] David Smith: Digital Transmission Systems, Springer- Macmillan India Ltd

Paper Code No : MEVS–713	**L**	**T**	**C**
Paper : MEMS and IC Integration	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Overview of CMOS process in IC fabrication, MEMS system-level design methodology: Overview of MEMS, Overview of Microsystems fabrication Processes, Bulk Micromachining, Surface micromachingin, LIGA Process, Microsystem Design: Design Considerations, Process design, Mechanical Design, Mechanical Design using FEM, CAD.

Unit 2

Equivalent Circuit representation of MEMS, : working principles of Microsystem, scaling laws in miniaturatization, materials for MEMS and Microsystem, signal-conditioning circuits and sensor noise calculation.

Unit 3

Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer, Gyroscope, RF MEMS switch with electronics.

Unit 4

Bolo meter design. RF MEMS : Introduction to RF MEMS, Elements of RF circuit Design, Material and application of RF MEMS and Optical MEMS.

Text Books:

[T1] Gregory T.A. Kovacs, Micromachined Transducers Sourecbook, The McGraw-Hill, Inc. 1998
[T2] Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
[T3] Nadim Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
[T4] M.H. Bao, Micro Mechanical Transducers, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
[T5] H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.

Reference Books

[R1] Masood Tabib-Azar, Microactuators, Kluwer, 1998.
[R2] Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994
[R3] D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997
[R4] James M.Gere and Stephen P. Timoshenko, Mechanics of Materials, 2nd Edition, Brooks/Cole Engineering Division, 1984

Paper Code No : MEVS – 715 **L T C**
Paper : Network on Chip Design **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Basic Concepts of Network-on-Chip [T1] : Introduction to interconnection networks, Walk through of a simple network, Topology basics, Constraints and measures, Butterfly networks, Cube networks. Concentration and slicing, Non-blocking topologies, Topology overflow and wrapup, Routing basics and taxonomy, Oblivious routing. Adaptive routing, Routing mechanics

Unit 2

Flow Control and Deadlock T1]: Flow control basics. Resources and allocation strategies, Circuit switching. Store and forward. Dropping flow control. Misrouting. Cut through. Wormhole flow control, Virtual channels. Deadlock and livelock. Principles of deadlock. Buffer deadlock and channel deadlock. Deadlock in cyclic networks. Inter-dimension deadlock. Avoiding deadlock with virtual channels. The turn models.

Unit 3

Router Micro-architecture [T1]: Basic router. Input buffers and buffer organization. Internal switch organization: crossbars, dimension-ordered, and multistage, Router datapath components, router pipelining, router delay Models, Allocators. Arbiters. The allocation problem - allocating VCs to packets and bandwidth to flits. Bipartite matching. Naïve allocation. Separable allocators. Wavefront allocation.

Unit 4

Network Performance Analysis and Reliability [T1]: Network performance analysis, Analysis of networks with dropping flow control. Analysis of blocking, The effects of buffers, Simulation vs. analysis, The effect of traffic patterns, Load balance and route diversity, Definition of Reliability and Availability, Failure mechanisms and fault models, Path diversity, Pragmatics and self-healing

Text Books:

[T1] William J Dally, Principles and Practices of Interconnection Networks (The Morgan Kaufmann Series in Computer Architecture and Design) , Morgan Kaufmann; 1 edition (January 1, 2004)

Reference Books:

[R1] Sao-Jie Chen , Ying-Cherng Lan , Wen-Chung Tsai ,Yu-Hen Hu, Reconfigurable Networks-on-Chip, Springer; 2012 edition (December 15, 2011)

[R2] Tim Kogel, Rainer Leupers , Heinrich Meyr , Integrated System-Level Modeling of Network-on-Chip enabled Multi-Processor Platforms, Springer, 1st ed. 2006 edition (November 19, 2010)

[R3] Giovanni De Micheli , Luca Benini , Networks on Chips: Technology and Tools (Systems on Silicon), Morgan Kaufmann; 1 edition (August 3, 2006)

Paper Code No : MEVS – 717 **L T C**
Paper : CMOS RF Design **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1

Introduction : RF systems – basic architectures, Transmission media and
Reflections, Maximum power transfer.
Passive RLC Networks: Parallel RLC tank, Q , Series RLC networks, matching Pi match, T match. Passive IC Components: Interconnects and skin
Effect, Resistors, capacitors Inductors Review of MOS device.

Unit 2

Distributed Systems: Transmission lines, reflection coefficient, The wave equation,Lossy transmission lines, Smith charts – plotting gamma.
High frequency Amplifier design :Bandwidth estimation using open-circuit time constants Bandwidth estimation using short-circuit time constants Risetime, delay and bandwidth Zeros to enhance bandwidth Shunt-series amplifiers,
tuned amplifiers Cascaded amplifiers.

Unit 3

Noise :Thermal noise, flicker noise review Noise figure.
LNA Design: Intrinsic MOS noise parameters, Power match versus noise match Large signal performance, design examples & Multiplier based mixers
Mixer Design : Subsampling mixers.
RF Power amplifier design :Class A, AB, B, C amplifiers, Class D, E, F amplifiers RF Power amplifier.

Unit 4

VCO : Resonators Negative resistance oscillators. PLL Design : Linearized PLL models, Phase detectors, charge pumps, Loop filters, Frequency synthesis and oscillators : Frequency division, integer-N synthesis, Fractional frequency
Synthesis. Phase noise: General considerations. Radio architectures: GSM radio architectures, CDMA, UMTS radio architectures

Text Books

[T1] The Design of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee. Cambridge University Press, 2004.

[T2]RF Microelectronics by Behzad Razavi. Prentice Hall, 1997.

Reference Books:

[R1] B. Razavi “RF Microelectronics” PHI, 1998.
[R2] R. Jacob Baker, H.W. Li, D.E. Boyce “ CMOS Circiut Design, layout and Simulation” PHI,1998.
[R3] Y.P. Tsividis “Mixed Analog and Digital Devices and Technology”, TMH 1996.

Paper Code: MEVS – 719	L	T	C
Paper: Circuit Interconnections & Packaging for VLSI	4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Unit 1 [T1]

Microelectronics Interconnection : Signal transmission in interconnects, problems in interconnects, physical factors in interconnection design, On-Chip interconnection Technology, Scaling trends, Electrical reference connection scheme, Package level interconnection technology, scaling trends, power voltage distribution and switching noise.

Unit 2 [T1]

Interconnection Modeling: Physical foundation for circuit model of interconnections, TEM waves, Quasi-TEM Model, Simplification of RLGC Model, Lossless transmissions line model: resistive driver model, effect of signal rise time, CMOS driver with open circuit load, Lossy Transmission model: Effect of semiconductor substrate, optimum line model selection, Cross talk effect in digital circuits,

Unit 3 [T1]

Packaging Interconnects: Packaging structure, Body fabrication technology, External connections, chip connections, Lumped electrical parameter modeling of packages, calculation of circuit parameters, concept of partial conductance, skin effect calculations, Power distribution modeling from EM simulation

Unit 4[T1]

Simulation of package effect : effect of SSN, effect of crosstalk, techniques for avoidance of crosstalk, switching noise avoidance, Noise detection in logic circuits, ATPG for stuck-at fault, ATPG for crosstalk, other test techniques

Text Books:

[T1] Interconnection Noise in VLSI Circuits (Paperback), Francesc Moll, Miquel Roca, Springer; 2004 edition (December 14, 2011)

Reference Books:

[R1] Circuits, Interconnections, and Packaging for VLSI , H. B. Bakoglu , Addison-Wesley Pub (Sd) (January 1990)

Code No: MEVS-751	**L**	**P**	**C**
Lab-1	**-**	**2**	**1**

Experiment of the lab will be based on AVDA

Code No. : MEVS-753	**L**	**P**	**C**
Lab-2:	**-**	**2**	**1**

Experiment of the lab will be based on VLSI Testing.

Code No: MEVS-755*	**L**	**P**	**C**
Term paper-3		**-**	**2**

Lab Experiment/Lab- project will be based on Electives

*NUES: Non University Exam

Paper Code: MEVS - 757	**L**	**T**	**C**
Lab: Minor Project			**6**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

Code No: MEVS-752 **C**
Subject: Dissertation **24**

The student will submit a synopsis at the beginning of the semester for the approval from the school project committee in a specified format. Synopsis must be submitted within a two weeks. The first defense, for the dissertation work, should be held with in a one month. Dissertation Report must be submitted in a specified format to the school for evaluation purpose.

Code No: MEVS-754* **C**
Subject: Seminar & Progress Report **4**

The student will have to present the progress of the dissertation work through seminars and progress reports at the interval of four weeks.

Code No: MEVS-756* **C**
Subject: Term paper4 **2**

*NUES: Non University Exam

Paper Code: MEIT-608 **L T C**
Subject: Web Semantics **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Review of Internet and Web, it's origin and growth, W3C, various versions of Web, Limitations of present web, Semantic Web as the next generation web and it's various concerns. Semantic Web roadmap, it's need and goal, capabilities and limitations, various issues, applications.

UNIT – II

Tim Berner's Lee architecture of Semantic Web (various versions), it's various technologies and tools. Basic elements of HTML & XML, Examples, XML, XMLS, XML Query Language, RDF, RDFS, RDF/XML, URI, Cryptography concerns and issues. Programming and mathematical concerns.

UNIT – III

Ontology as a backbone for incorporating semantics and it's various significant concerns and issues, SPARQL Semantics execution and Query processing, optimization and execution along with implementation illustrations for filtering RDF using Jena and twinkle tool.

UNIT – IV

Significant concerns of Web Semantics like Semantic Web Services, Software agents, Search Engines, Information Extraction and Retrieval, Semantic Annotation, NLP, Web usage mining, Social Networks for Network Analysis and visualization etc.

TEXT BOOKS

1. Berners-LEE, Godel and Turing, "Thinking on the Web", Wiley, 2006.
2. Devedzic V, "Semantic Web Education", Springer, 2006
3. John Hebeler and Matthew Fisher, "Semantic Web Programming", Wiley, 2009
4. Karin Breitman and Marco," Semantic Web: Concepts, Technologies and Applications", 2009
5. Rajendra Akerkar, "Foundations of the Semantic Web:XML,RDF and Ontology",2009,Oxford.

REFERENCES

1. Geroimenko and Chen, "Visualizing the Semantic Web", Springer, 2004.
2. Passin, "Explorer's guide to the Semantic Web", Manning, 2004.
3. Pascal, Krotzsch and Rudolph, "Foundations of Semantic Web Technologies", SRC Press.
4. Grigoris Antoniou and Paul Groth, "A Semantic Web Primer", 2012
5. Peter, Gergely and Tamas, "The Semantic Web explained-the technology and mathematics behind web 3.0", Cambridge University Press, 2014.

Paper Code: MEIS-607	**L**	**T/P**	**C**
Subject: Advanced Operating System	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

UNIT – I

Competitive study of OS: UNIX, Multics.

UNIT – II

Unix file system -Measurements, The log- structured file system , server less Network file system , The coda file system.

UNIT – III

AFS, Virtual memory, user level virtual memory, software fault isolation , On -demand distillation . X - kernel , active message, Global network scheduling, Network optimization , synchronization scheduling .

UNIT – IV

Extensible operating system, issue of security in OS, cryptographic file system.

TEXT BOOKS/ REFERENCES:

1. A.S Tannenbaum, "Operating Systems Concept", Addition Wesley, 2002
2. Silbersachatz and Galvin, "Operating Systems Concept", Addition Wesley, 2002
3. Charles Crowley, "Operating Systems", Tata McGraw-Hill Edition
4. Branch Hansen.P , "Operating Systems Principles",Prentice-Hall,1973
5. Tannenbaum, A.S, "Modern Operating Systems", Pearson,2007